IN THE CLAIMS:

Please amend the claims as follows.

1. (Original) An instruction segment storing method, comprising:

building an instruction segment,

determining whether the instruction segment satisfies a filtering condition, and

if the instruction segment satisfies the filtering condition, storing the instruction segment in a segment cache.

2. (Currently amended) The method of claim 1, wherein the filtering condition may be met only if all instructions in the instruction segment were assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

3. (Currently amended) The method of claim 1, wherein the filtering condition may be met only if at least one instruction in the instruction segment was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

4. (Original) The method of claim 1, wherein the filtering condition may be met only if a predetermined number of instructions in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

5. (Original) The method of claim 1, wherein the filtering condition may be met only if an instruction of the segment by which the segment is to be indexed was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

6. (Currently amended) An instruction segment storing method, comprising:

building an instruction segment,

determining, from location flags associated with ~~instruction~~instructions in the instruction segment, whether the instruction segment satisfies a filtering condition, and

if so, storing the instruction segment in a segment cache.

7. (Currently amended) The method of claim 6, wherein the filtering condition may be met only if all instructions in the instruction segment were assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

8. (Currently amended) The method of claim 6, wherein the filtering condition may be met only if at least one instruction in the instruction segment was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

9. (Currently amended) The method of claim 6, wherein the filtering condition may be met only if a predetermined number of instructions in the instruction segment were assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

10. (Original) The method of claim 6, wherein the filtering condition may be met only if an instruction of the segment by which the segment is to be indexed was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

11. (Original) A front end system for a processing agent, comprising:

an instruction cache system, and

an instruction segment system, comprising:

a segment cache, and

a segment builder provided in communication with the instruction cache system, to store a new instruction segment in the segment cache when a filtering condition is met.

12. (Original) The front end system of claim 11, further comprising a history map provided in communication with the segment builder to identify when the filtering condition is met.

13. (Original) The front end system of claim 12, wherein the history map is a direct mapped cache.

14. (Original) The front end system of claim 12, wherein the history map is a set associative cache.

15. (Original) The front end system of claim 14, wherein the history map comprises a plurality of cache entries having a width corresponding to a width of a tag address of an instruction pointer in the system.

16. (Original) The front end system of claim 14, wherein the history map comprises a plurality of cache entries having a width corresponding to a width of a portion of a tag address of an instruction pointer in the system.

17. (Original) The front end system of claim 11, wherein the instruction cache system outputs instructions and location flags to the segment builder, the segment builder determining whether the filtering condition is met based on location flags associated with instructions of the new instruction segment.

18. (Original) A processing agent, comprising:

a cache hierarchy, and

a front end system comprising:

an instruction cache system in communication with the cache hierarchy, and

an instruction segment system, comprising:

a segment cache, and

a segment builder provided in communication with the instruction cache system, to store a new instruction segment in the segment cache when a filtering condition is met.

19. (Original) The processing agent of claim 18, further comprising a history map provided in communication with the segment builder to identify when the filtering condition is met.

20. (Original) The processing agent of claim 18, wherein:

the instruction cache system outputs instructions and location flags to the segment builder, the location flags distinguishing instructions retrieved from the instruction cache system from instructions retrieved from the cache hierarchy, and

the segment builder determining whether the filtering condition is met based on location flags associated with instructions of the new instruction segment.

21. (Original) A computer system, comprising the processing agent of claim 18, wherein the cache hierarchy includes an internal cache and a system memory.

22. (Original) A computer system, comprising the processing agent of claim 18, wherein the cache hierarchy includes an internal cache and an external cache.

Please add the following new claims:

23. (New) A method, comprising:

building an instruction segment,

determining whether the instruction segment satisfies a filtering condition, and

storing the instruction segment in a segment cache unless the instruction segment does not satisfy the filtering condition.

24. (New) The method of claim 23, wherein the determining comprises determining whether all instructions in the instruction segment were assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

25. (New) The method of claim 23, wherein the determining comprises determining whether at least one instruction in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

26. (New) The method of claim 23, wherein the determining comprises determining whether a predetermined number of instructions in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

27. (New) The method of claim 23, wherein the determining comprises determining whether an instruction of the segment by which the segment is to be indexed was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

28. (New) The method of claim 23, wherein the determining comprises determining whether the instruction segment has been built at least twice.

29. (New) The method of claim 23, wherein the determining comprises comparing location flags identifying locations from which instructions within the segment were retrieved to a predetermined filtering condition.

30. (New) A front end system for a processing agent, comprising:

an instruction cache system, and

an instruction segment system, comprising:

a segment builder to build instruction segments from instructions retrieved from the instruction cache system,

a segment cache to store instruction segments unless the instruction segments fail a filtering condition.

31. (New) The front end system of claim 30, further comprising a history map provided in communication with the segment builder to identify when the filtering condition is met.

32. (New) The front end system of claim 31, wherein the history map is a direct mapped cache.

33. (New) The front end system of claim 31, wherein the history map is a set associative cache.

34. (New) The front end system of claim 33, wherein the history map comprises a plurality of cache entries having a width corresponding to a width of a tag address of an instruction pointer in the system.

35. (New) The front end system of claim 33, wherein the history map comprises a plurality of cache entries having a width corresponding to a width of a portion of a tag address of an instruction pointer in the system.

36. (New) The front end system of claim 30, wherein the instruction cache system outputs instructions and location flags to the segment builder, the segment builder determining whether the filtering condition is met based on location flags associated with instructions of the new instruction segment.